

COMPLETE LISTING OF THE CLAIMS

The following lists all of the claims that are or were in the above-identified patent application.

1. (Previously Presented) A probing system for testing a device comprising:
a probe comprising a semiconductor die and probe tips on the semiconductor die,
wherein the probe tips comprise bumps that are arranged in a pattern that matches a pattern of terminals on the device and that directly contact the terminals during testing of the device, the probe tips being affixed to the semiconductor die so that the pattern of the probe tips expands/contracts with thermal expansion/contraction of the semiconductor die; and
a tester electrically connected to the probe tips.
2. (Original) The system of claim 1, wherein the device comprises a semiconductor material that is substantially the same as material in the semiconductor die.
3. (Original) The system of claim 1 further comprising a probe card including a receptacle in which the probe is detachably mounted, wherein the tester makes electrical connections to the probe tips through the probe card.
4. (Original) The system of claim 3, wherein the probe further comprises a substrate on which the semiconductor die is mounted, the receptacle being sized to hold the substrate.
5. (Original) The system of claim 4, wherein the substrate is substantially identical to a substrate used in a flip-chip package for the device.
6. (Original) The system of claim 4, wherein the semiconductor die comprises contact pads to which respective probe tips are attached, and wire bonds electrically connect the contact pads to the substrate.
7. (Original) The system of claim 1, wherein the semiconductor die comprises:
terminals on a bottom surface of the semiconductor die; and
conductive vias that pass through the semiconductor die and provide electrical

connections between the probe tips on a top surface of the die and the terminals on the bottom surface.

8. (Original) The system of claim 7, wherein the probe further comprises a substrate on which the semiconductor die is mounted, wherein the terminals of the semiconductor die directly contact the substrate.

9. (Original) The system of claim 8, further comprising a probe card, wherein terminals on the substrate directly contact the probe card.

10. (Original) The system of claim 1, further comprising a positioning system adapted to position the probe relative to the device so that the probe tips contact the terminals on the device.

11. (Canceled)

12. (Canceled)

13. (Currently Amended) A method for forming a probe for electrical testing of a semiconductor device, comprising:

forming probe tips on a semiconductor die in a pattern matching a pattern of terminals on the semiconductor device, wherein forming the probe tips comprises:

forming contact pads on the semiconductor die; and

forming conductive bumps on a surface of the contact pads, wherein tops of the conductive bumps provide surfaces that during testing directly contact the terminals of the semiconductor device; and

fabricating an interconnect structure for electrical connection of the probe tips to test equipment.

14. (Canceled)

15. (Original) The method of claim 13, wherein fabricating the interconnect structure comprises forming conductive traces on a surface of the semiconductor die on which the probe tips reside.

16. (Original) The method of claim 15, further comprising wire bonding the conductive traces to a substrate.

17. (Original) The method of claim 13, wherein fabricating the interconnect structure comprises forming conductive vias through the semiconductor die, the vias respectively being in electrical contact with the probe tips.

18. (Previously Presented) The method of claim 17, wherein forming the conductive vias comprises:

forming holes in the semiconductor die; and
filling the holes with a conductive material.

19. (Previously Presented) The method of claim 18, wherein forming the holes comprises laser drilling.

20. (Previously Presented) The method of claim 18, wherein forming the holes comprises etching.

21. (Previously Presented) The method of claim 17, wherein forming the conductive vias comprises forming doped regions that extend through the semiconductor die.

22. (Previously Presented) The method of claim 17, further comprising forming terminals in contact with the vias on a surface of the semiconductor die opposite of a surface on which the probe tips reside.

23. (Previously Presented) The method of claim 22, further comprising attaching the terminals to an interconnect substrate.

24. (Previously Presented) The method of claim 23, wherein attaching the terminals comprises performing a solder reflow process.

25. (Previously Presented) The method of claim 13, wherein forming probe tips

further comprises planarizing the bumps.

26. (Previously Presented) The method of claim 25, wherein planarizing comprises chemical mechanical polishing of the bumps.

27. (Previously Presented) The method of claim 13, forming contact pads on the semiconductor die comprises a manufacturing process that is substantially identical to a process used in fabricating contact pads on the semiconductor device to be tested.

28. (Previously Presented) The method of claim 27, wherein the manufacturing process uses a mask that is substantially identical to a mask used in fabricating the contact pads on the semiconductor device to be tested.

29. (Previously Presented) The system of claim 1, further comprising contact pads on the semiconductor die, wherein the bumps respectively reside on the contact pads.

30. (Previously Presented) The system of claim 29, wherein the contact pads have a pattern identical to corresponding contact pads on the device tested.

31. (Previously Presented) The system of claim 1, wherein surfaces of the bumps that contact the device are planar and in the same plane.

32. (Previously Presented) The system of claim 1, wherein the semiconductor die is substantially identical to the device.

33. (Previously Presented) The system of claim 1, wherein the bumps are of a type suitable for use in a flip-chip package.